

PA 1042299

PCT / IB 04 / 01851

14 JUN 2004

14 JUN 2004

PCT

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

July 22, 2003

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE UNDER 35 USC 111.

APPLICATION NUMBER: 60/477,542

FILING DATE: June 11, 2003

PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH RULE 17.1(a) OR (b)

By Authority of the
COMMISSIONER OF PATENTS AND TRADEMARKS



E. Bornett
E. BORNETT

Certifying Officer

BEST AVAILABLE COPY

06/11/03
17231 U.S. PTO

Please type a plus sign (+) inside this box →

+

06-12-03

60477542 .061103

PTO/SB/15 (02/01)

Approved for use through 10/31/2002. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53 (c).

Express Mail Label No. EV 335 816 676

Date of Deposit: JUNE 11, 2003

INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
THEODORE	LETAVIC	PUTNAM VALLEY, NY

☐ Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (280 characters max)

"HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS"

CORRESPONDENCE ADDRESS

Direct all correspondence to:

☒ Customer Number

24737

OR

Type Customer Number here

24737

☒

Firm or
Individual Name

U. S. PHILIPS CORPORATION

Address

P. O. BOX 3001

Address

City

BRIARCLIFF MANOR

State

NY

ZIP

10510

Country

USA

Telephone

(914) 945-6000

Fax

(914) 332-0615

ENCLOSED APPLICATION PARTS (check all that apply)

☒ Specification Number of Pages

7

☐ CD(s), Number

X Drawing(s) Number of Sheets

3

X Other (specify)

IDS

☐ Application Data Sheet. See 37 CFR 1.76

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT (check one)

☐ Applicant claims small entity status. See 37 CFR 1.27.

☐ A check or money order is enclosed to cover the filing fees

☒ The Commissioner is hereby authorized to charge filing fees or credit any overpayment to Deposit Account Number:

14-1270

FILING FEE
AMOUNT (\$)

160.00

☐ Payment by credit card. Form PTO-2038 is attached.

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No.

☐ Yes, the name of the U.S. Government agency and the Government contract number are: _____

Respectfully submitted,

SIGNATURE

Steven R. Biren

Date 6/11/03

REGISTRATION NO.: 26,531

(if appropriate)

Docket Number: US030162

TYPED or PRINTED NAME

STEVEN R. BIREN

TELEPHONE

(914) 333-9830

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is used by the public to file (and by the PTO to process) a provisional application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the complete provisional application to the PTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Box Provisional Application, Assistant Commissioner for Patents, Alexandria, VA 22313.

17613 U.S. PTO
60/477542

HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS

TECHNICAL FIELD

This invention relates to CMOS devices, and more specifically, to a technique of achieving elimination of the parasitic MOS channel present in thin film CMOS devices configured in the source, or what is called the source follower, configuration. Also disclosed is a methodology of performing a deep N implant in order to effectuate the inventive structure. Although most applicable in PMOS devices, the invention may also be utilized in the NMOS configuration.

10

BACKGROUND AND SUMMARY OF THE INVENTION

Figure 1 shows a thin film CMOS device including a source 101, drain 102, and MOS gate region 103. The SOI layer 104 forms an MOS junction 105 with an buried oxide layer 106. Below buried oxide layer 106 is a substrate layer 107, which would typically be several hundred microns thick. On the scale shown in Figure 1, the substrate layer 107 is too thick to depict and thus is not fully shown.

In source follower mode, sometimes called source high mode, the source 101 is biased with a voltage that is typically higher than the voltage at which substrate 107 is kept. This voltage difference could be over two hundred volts in typical applications. In thin film devices where the SOI layer 104 may be only slightly more than a micron thick, this voltage difference may be sufficient to induce an unwanted depletion region at or near the MOS junction 105. As shown therefore in Figure 1, a parasitic path 110 between source 101 and drain 102 exists at the MOS junction. This region creates a parasitic MOS channel, allowing leakage current to be conveyed between the source 101 and drain 101

when the real MOS gate region 103 is intended to be turned off. The device thus undesirably acts as if a second gate region existed, wherein the second gate is in the on state even when the actual gate region 103 is in the off state.

To date, there exists no known solution for stopping this leakage current when thin film SOI devices are utilized in the source follower configuration. Prior solutions all involve use of a much thicker SOI layer 104, rather than thin film devices. These prior devices have such a thick SOI layer that the depletion region resulting in the parasitic MOS channel 110 does not occur. However, in thin film applications the region 110 acts as a second current path in addition to the normal gate region.

There exists a need in the art for a technique of eliminating this parasitic channel 110 in source follower configurations with thin film SOI devices.

In complimentary arrangements, (i.e. using NMOS devices in which the source is biased much lower than the substrate) a similar problem may exist.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a depiction of a prior art CMOS thin film device, showing a parasitic MOS channel 110;

Figure 2 is a conceptual depiction of a device fabricated in accordance with the present invention; and

Figures 3A – D depict doping concentrations at various locations throughout the device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 2 depicts an exemplary PMOS device including the deep N layer 201 placed
5 below the source region 101. A substrate region 107 is maintained at an exemplary voltage of
-200, over 200 volts lower than the typical voltage at which the source is biased. Due to the
relatively thin SOI layer 104, (slightly more than 1 micron) a parasitic MOS channel 110
results from a depletion region that forms between the drain 102 and source 101 as indicated in
Figure 1. However, the deep N layer 201 shown directly below the source region 101 prevents
10 full depletion and instead forms the space charge neutral region 205 as indicated in dotted
outline in Figure 2. This space charge neutral region 205 prevents current flow between the
source 101 and drain 102 along any parasitic channel than may otherwise be formed across
MOS channel 110.

In the preferred embodiment, the implantation of the deep N layer 201 should be
15 accomplished using a doubly ionized implant of 31P++ and a 200 KeV implant machine. This
gives 400 KeV implant energy, without the need for a high energy implant machine.

It is also noted that while the deep N layer is shown below the source region 101 in
Figure 2, it is noted that the space charge neutral region 205 may be implemented anywhere
along what would otherwise be the parasitic current path 110 between the source 101 and drain
20 102. Thus, the deep N layer 201 may be placed directly below drain region 102, rather than
below source region 101.

While the device has principal application in source high PMOS configurations, the
complimentary device may be implemented in NMOS as well. Such an MMOS device would
involve the P implant below the source or drain in similar concentration to those already

described, and would be applicable in arrangements where the bias configuration of the device is the reverse of what has been described herein with respect to PMOS devices.

Figures 3A – D show further manufacturing information regarding the implementation of the present invention in a PMOS device. Fig. 3A depicts a cross section showing the relative thickness' of the various portions of the device previously described. The device depicted in 3A is doped in concentrations profiled in Figure 3B. Note that Figures 3C and 3D compare the doping concentrations present in the source and drain regions respectfully. Note the concentration of the doping in the deep N region is shown in Figure 3D as being approximately 1 order of magnitude higher than the concentration shown in Figure 3B for the Nwell, the gate region.

It is noted that while the above describes the preferred embodiment of implementing the invention, various modifications and additions will be apparent for those that are skilled in the art. Such modifications are intended to be covered by the claims appended hereto.)

WHAT IS CLAIMED IS:

1. A thin film Silicon on Insulator (SOI) device comprising a source, a gate, a drain,
an SOI layer, and a substrate layer, the substrate layer being maintained at a potential
5 enough lower than the source so that a parasitic MOS channel is formed between the source
and drain; and a Deep N implant layer formed between either the source or drain and the
parasitic MOS channel to prevent the flow of current between the source and drain via the
parasitic MOS channel when the device is in an off state.
- 10 2. The device of claim 1 wherein the Deep N implant layer is formed between the
source and the parasitic MOS channel.
3. The device of claim 1 wherein the Deep N implant layer is formed between the
drain and the parasitic MOS channel.
- 15 4. A thin film Silicon on Insulator (SOI) device comprising a source, a gate, a drain,
an SOI layer, and a substrate layer, the SOI layer being maintained at a potential enough
higher than the source so that a parasitic MOS channel is formed between the source and
drain; and a Deep P implant layer formed between either the source or drain and the
20 parasitic MOS channel to prevent the flow of current between the source and drain via the
parasitic MOS channel when the device is in an off state.
5. The device of claim 1 wherein the Deep P implant layer is formed between the
source and the parasitic MOS channel.
- 25 6. The device of claim 1 wherein the Deep P implant layer is formed between the
drain and the parasitic MOS channel.
7. A method of isolating the source and drain of an MOS device to avoid a parasitic
30 MOS channel being formed comprising adding a double ionized 31P++ implant to form a
deep N layer beneath the drain or source of the MOS device, thereby preventing current

flow across a parasitic MOS channel formed in said MOS device when the device is in an off state.

- 5 8. The method of claim 7 wherein said device includes a buried oxide layer, and wherein said parasitic MOS channel forms at or near the buried oxide layer – silicon layer interface.
- 10 9. The method of claim 7 wherein the doping concentration of the deep N layer is approximately one order of magnitude higher than that of the NWell layer on the device.
- 15 10. A CMOS device comprising source and drain regions adjacent to a buried oxide layer and separated by a gate region, the buried oxide layer being adjacent to a substrate layer, and an implant layer of particles directly below the drain or source such that when the difference in potential between the substrate and the source exceeds 200 volts, a parasitic MOS channel is induced across the gate region and the implant layer isolates said parasitic MOS channel from said drain region to thereby prevent current flow between said source and drain via said parasitic MOS channel.
- 20 11. The device of claim 10 wherein the ionized particles are implanted using approximately 200keV of energy.

25

ABSTRACT

5 An Silicon on Insulator device is disclosed wherein a parasitic channel induced in a thin film portion of the device is prevented from allowing current flow between the source and drain by a Deep N implant directly below the source of drain. The deep N implant prevents a depletion region from being formed, thereby cutting off current flow between the source and the drain that would otherwise occur.

10

15

Approved for use through 10/31/2002. OMB 0651-0032
 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
 Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63) <input checked="" type="checkbox"/> Declaration Submitted With Initial Filing OR <input type="checkbox"/> Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)	Attorney Docket Number	PHUS030162WO
	First Named Inventor	THEODORE LETAVIC
	COMPLETE IF KNOWN	
	Application Number	/
	Filing Date	
	Group Art Unit	
	Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS

the specification of which (Title of the Invention)

☒ is attached hereto
 OR
☐ was filed on (MM/DD/YYYY) [] as United States Application Number or PCT International Application Number [] and was amended on (MM/DD/YYYY) [] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached?	
				YES	NO
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

[Page 1 of 2]

Burden Hour Statement: This form is estimated to take 21 minutes to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Approved for use through 10/31/2002. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

DECLARATION — Utility or Design Patent Application

Direct all correspondence to:		<input checked="" type="checkbox"/> Customer Number or Bar Code Label		*24737*		OR		<input checked="" type="checkbox"/> Correspondence address below	
Philips Electronics North America Corporation									
Name									
P.O. BOX 3001									
Address									
BRIARCLIFF MANOR				NY		10510			
City				State		ZIP			
U.S.A.						(914)945-8000		(914) 332-0615	
Country						Telephone		Fax	
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.									
NAME OF SOLE OR FIRST INVENTOR:				<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])				THEODORE		Family Name or Surname			
						LETAVIC			
Inventor's Signature						Date			
PUTNAM VALLEY				NY		USA		USA	
Residence: City				State		Country		Citizenship	
25 BELL HOLLOW ROAD									
Mailing Address									
PUTNAM VALLEY				NY		10579		USA	
City				State		Zip		Country	
NAME OF SECOND INVENTOR:				<input type="checkbox"/> A petition has been filed for this unsigned inventor					
Given Name (first and middle [if any])				Family Name or Surname					
Inventor's Signature						Date			
Residence: City				State		Country		Citizenship	
Mailing Address									
City				State		Zip		Country	
<input type="checkbox"/> Additional Inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.									

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
In re Application of Atty. Docket

THEODORE LETAVIC

US030162

Serial No.

Filed: CONCURRENTLY

Title: HIGH-SIDE CMOS IN AN INTEGRATED SOI PROCESS

Commissioner for Patents
Alexandria, VA 22313

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:

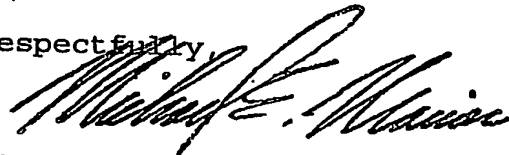
STEVEN R. BIREN

(Registration No. 26,531)

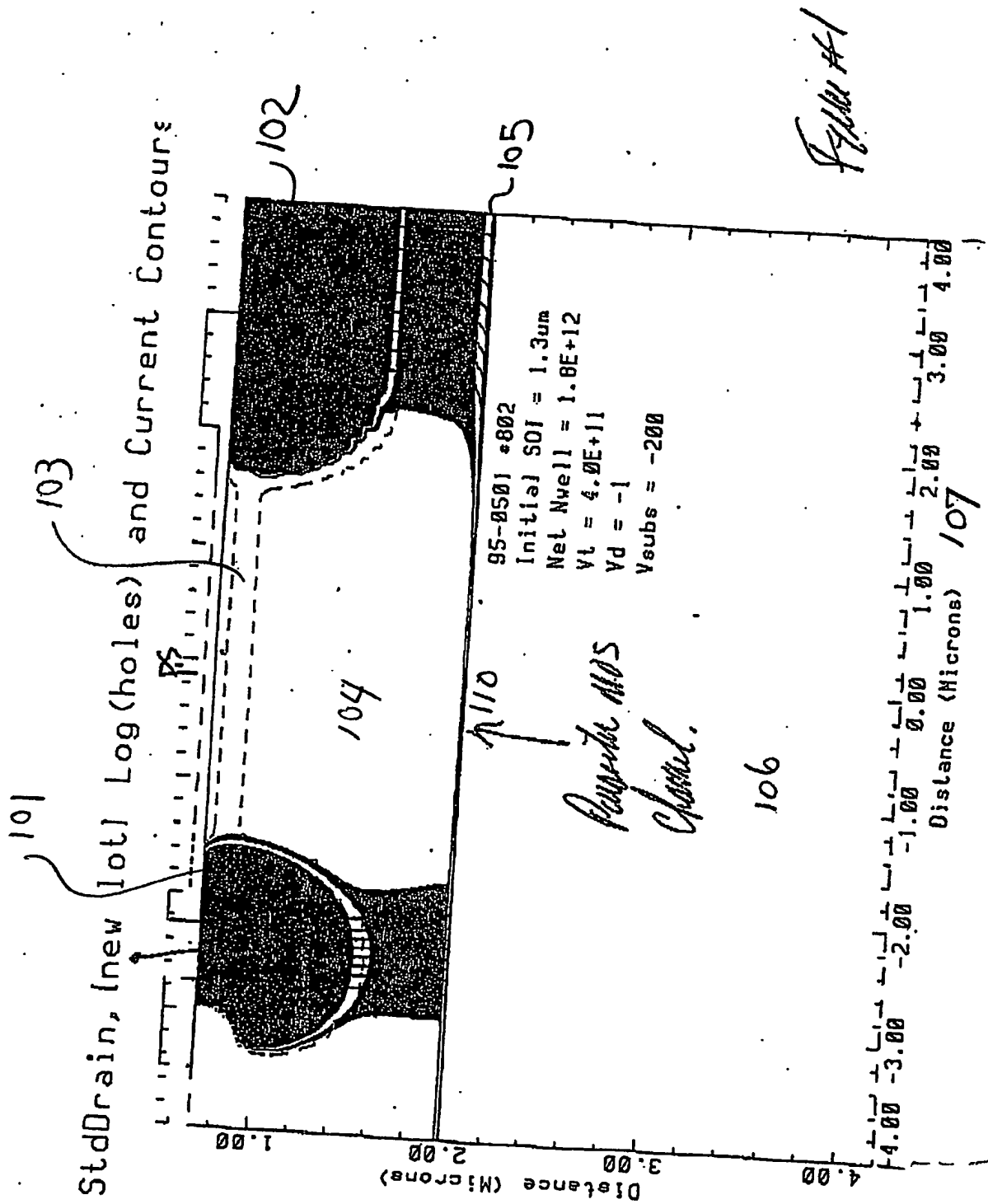
c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

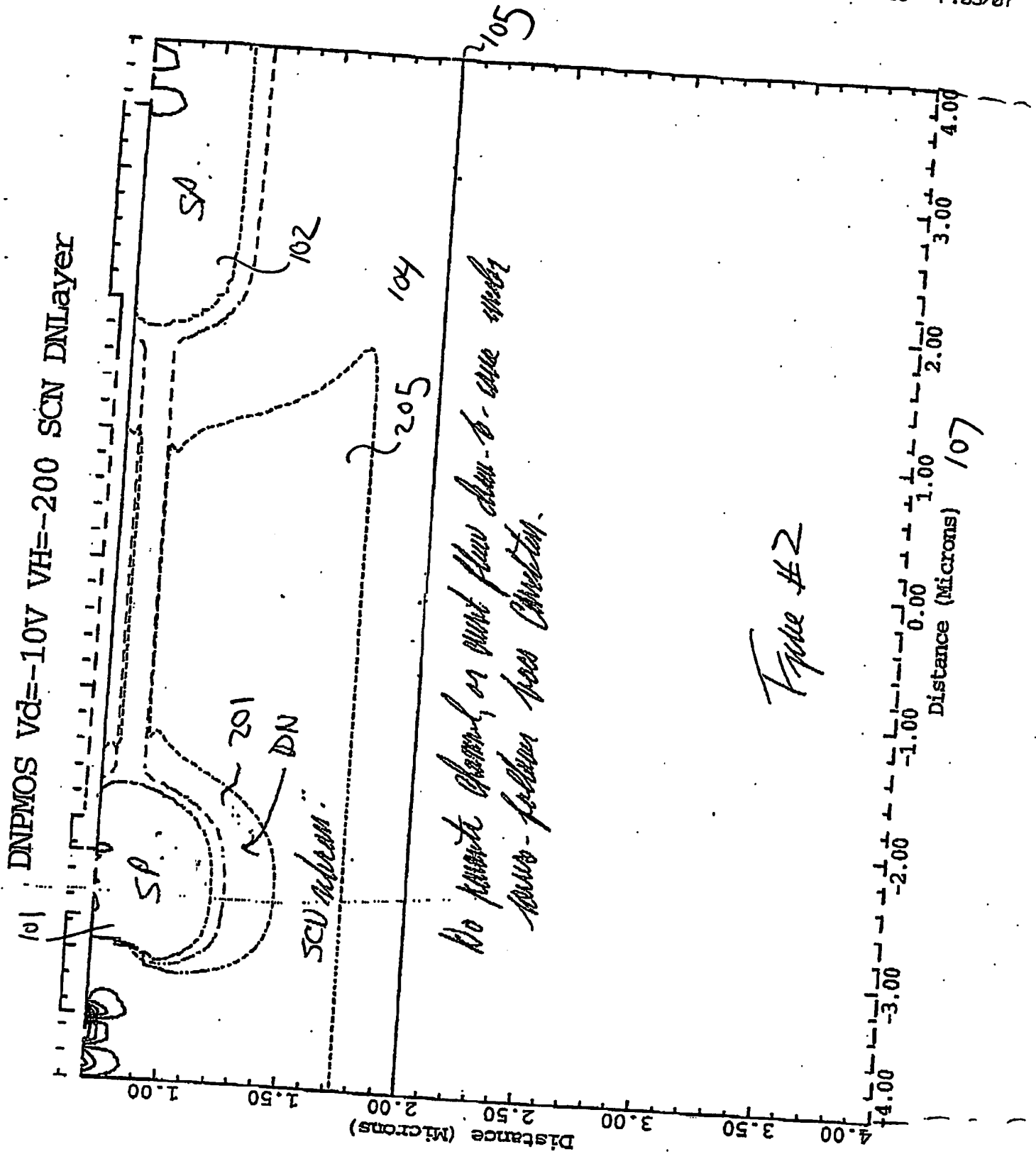
ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,



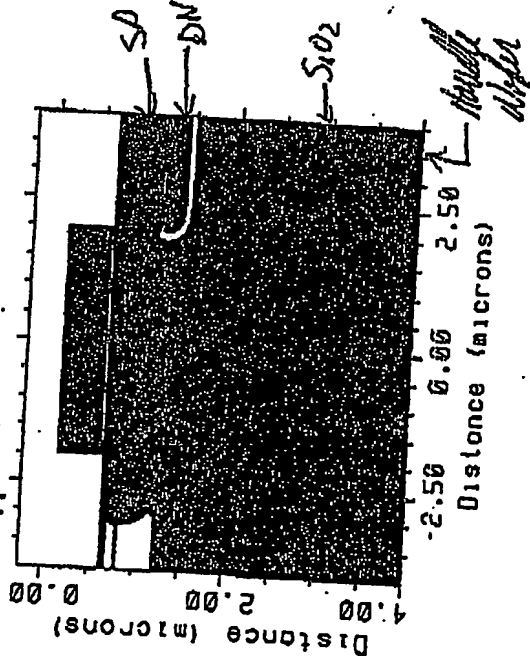
Michael E. Marion, Reg. 32,266
Attorney of Record



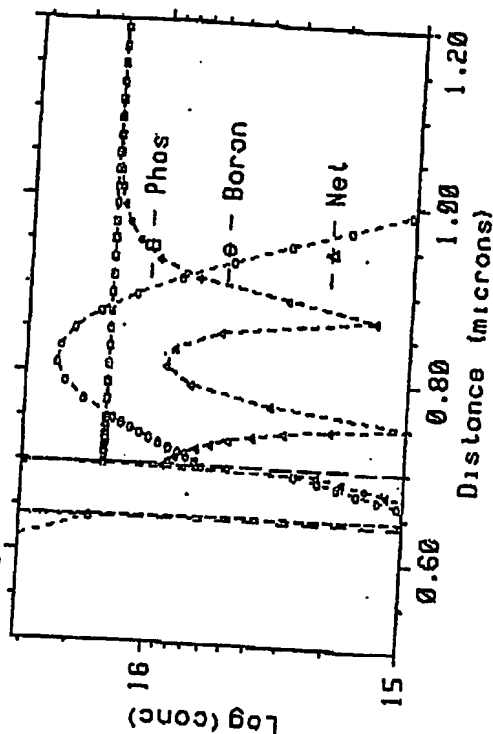


PMOS 400keV 5e12 1e15SP Xgrid

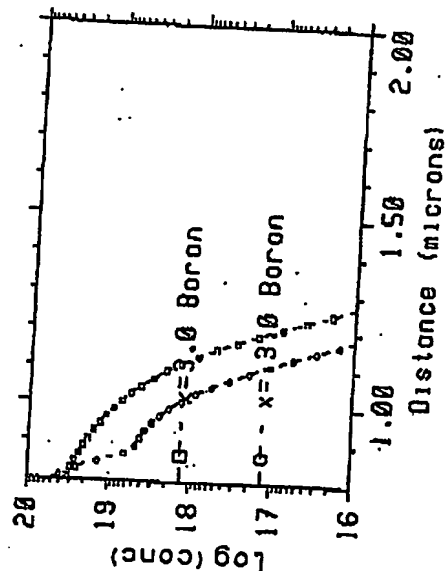
A



B Gate Profile



C SP Dope 1e15



D Drain Doping Net

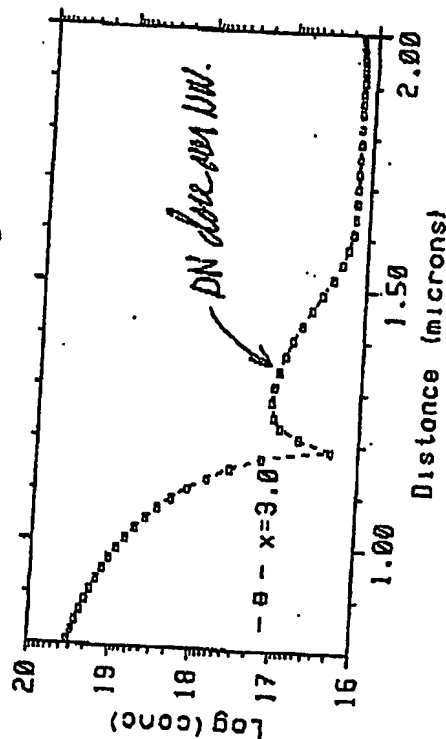


Figure #3

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

☒ **BLACK BORDERS**

☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**

☐ **FADED TEXT OR DRAWING**

☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**

☐ **SKEWED/SLANTED IMAGES**

☐ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**

☐ **GRAY SCALE DOCUMENTS**

☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**

☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**

☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.